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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,334	01/15/2002	Vishnu K. Agarwal	MI22-1913	7861

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EXAMINER	
NGUYEN, TUAN H	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,334	AGARWAL ET AL.	
	Examiner	Art Unit	
	Tuan H. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-21, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Schugraf et al..

With respect to claims 16, 27, Schugraf et al., figs. 3-5 and text on col.3-5 teaches the claimed capacitor construction including a surface area enhancement layer 20b formed from undoped rugged polysilicon over a substrate 10, the enhancement layer 20b having an outer surface area per unit area (top surface) that is greater than an inner surface area per unit area (bottom surface) of the enhancement layer 20b (fig. 3 and text on col. 4, second paragraph); a first capacitor electrode 30 over the enhancement layer 20b, the first capacitor electrode 30 having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate 10, and the first electrode 30 not comprising the enhancement layer 20b since the polysilicon layer 20 and subsequently formed

enhancement layer 20b is undoped. Note on col. 4, third paragraph for the step of forming thin conductive layer 30 from a doped polysilicon.

Schugraf et al. teaches the steps of increasing surface area of the first capacitor electrode for a DRAM, a capacitor dielectric and a second capacitor electrode over the dielectric, are inherently included in the capacitor for a DRAM structure.

With respect to claim 17, see col. 4, line 55 for the use of TiN in forming the first electrode.

With respect to claim 18, fig. 4 and text on col. 4, third paragraph shows enhancement layer 20b is a rugged polysilicon formed over the substrate 10, and the first electrode 30 being over the rugged polysilicon.

With respect to claims 19, 20 col. 4, second paragraph discloses the formation if polysilicon layer 20 and subsequently annealing to form spaced apart, rugged polysilicon 20b without doping.

With respect to claim 21, fig. 4 clearly shows the outer surface area of the first electrode 30 is at least 30% greater than the substrate outer surface 10 which is flat.

Claims 16, 18-24, 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Chi.

Chi, figs. 1-4 and related text on col. 2-3 teaches the claimed capacitor construction including an opening 113 in an insulating layer 111 over the substrate 101; a HSG surface area enhancement layer 203 over the sides of the opening but not over the bottom, the enhancement layer 203 having an outer surface area per unit area (top

surface) that is greater than an inner surface area per unit area (bottom surface) of the enhancement layer 203 (fig. 2); a conformal first capacitor electrode 301 over the enhancement layer 203 but not comprising the enhancement layer 203 since it is completely oxidized (col. 3, second paragraph); the first capacitor electrode 301 being sufficiently thin that it has a rugged outer surface with an outer surface area per unit area greater than an a surface area per unit area of the sides of the opening over which the HSG polysilicon layer is formed; a capacitor dielectric layer 401 and a second capacitor electrode 403 formed over the first electrode as shown in fig. 4.

With respect to claim 29, fig. 3 shows the first electrode 301 also has an inner surface area per unit area that is greater than the surface area per unit area of the sides of the opening.

Claims 16, 18-21, 27, are rejected under 35 U.S.C. 102(e) as being anticipated by Al-Shareef et al..

Al-Shareef et al., figs. 12-13 clearly show the claimed capacitor structure including a first capacitor electrode 144 over the HSG polysilicon enhancement layer 142. Al-Shareef et al. , col. 5, lines 39-41 defined layer 148 as an electrode; therefore, the electrode does not comprising the enhancement layer 142 as required by the claimed language, regardless of whether the enhancement layer is conductive or not; a high-k capacitor dielectric layer 152; and a second capacitor electrode 154 are formed over the first capacitor electrode 148.

With respect to claim 19, since no dopant is introduced in the formation of HSG polysilicon as disclosed on col. 5, third paragraph, therefore, it is considered as undoped.

With respect to claims 18, 20, 21 an HemiSpherical-Grain polysilicon inherently includes spaced apart grains to form a rugged polysilicon, and the first electrode 148 being over the rugged polysilicon 142 wherein the outer surface area of the first electrode 148 is at least 30% greater than the outer surface area of the substrate 126.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Background of the invention in view of Schugraf et al..

Background of the invention, pages 1-2 discloses the conventional capacitor in electronic circuits including HSG bottom electrode to increase surface area which in turns, increase capacitance.

With respect to the high dielectric constant material for capacitor as claimed in claim 26, see Background of the invention, page 1, last paragraph.

Background of the invention fails to teach the use of HSG for increasing surface area of the bottom electrode formed in a subsequent step.

Schugraf et al., as explained above, and shown in figs. 4-5 and related text, teaches the bottom capacitor layer 30 having an increased surface area over the HSG layer 20b in a capacitor structure.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the teaches from Schugraf et al. in Background of the invention for obtaining a capacitor bottom electrode structure having an increased surface area without any problems associated with oxidizing HSG bottom electrode from the conventional capacitor structure.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tu et al., Li et al., Ping et al., and Agarwal et al.'583 disclose capacitors having an increasing surface area of the bottom electrode.

Response to Arguments

Applicant's arguments filed 7/11/05 have been fully considered but they are not persuasive. Since Al-Shareef et al. clearly defined on col. 5, lines 39-41 that layer 148 is a first electrode, therefore the first electrode does not comprises the HSG enhancement layer 142 as the instant claims call for. Note that "the first electrode not comprising the enhancement layer" does not mean that the enhancement layer has to be undoped or insulated.

Secondly, since the HSG is undoped as disclosed on col. 5, third paragraph, therefore, the electrode does not comprise the enhancement layer 142 as interpreted by

the applicant. Note that the undoped polysilicon is never functioned as an insulating layer to block the current since it is thin (sub-micron), rugged (spaced apart grains), and semiconductor, not an insulator, therefore the current can still get through.

Contrary the applicant's argument in his Remarks, page 4 that the HSG from Al-Shareef et al. must be doped, or must be a conductive in order to performed the function as intended. For the reason as noted above and Applicant's attention is also directed to the cited reference to Tu et al., fig. 3, insulating layer 70 and related text on col. 3, lines 15-22, 27-30 for supporting the conclusion that even the layer is insulated, it still conducts (let the current go through) current. The same thing is happened in Al-Shareef et al.' device when the rugged HSG layer 142 is too thin, and having spaced-apart grains formed between the fist electrode 148 and the contact plug 143, it does not have to be conductive in order to conduct current.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813